T5289

Features

- **4.5V to 40V Input Range**
- **Continuous current (typ): 7A**
- **N-channel on-resistance (typ): 15mohm**
- **En/Fault functions**
- **Programmable over voltage lockout**
- **Internal under voltage lockout**
- **Short-circuit limit**
- **Programmable overload current limit up to 9A**
- **Controlled output voltage ramp**
- **Programmable soft start function**
- **Thermal latch (typ): 165°C**
- **Operating junction temp. - 40°C to 125°C**
- **Available in DFN10 (3x3 mm) package**

Applications

- **Fast Charging Cable**

General Description

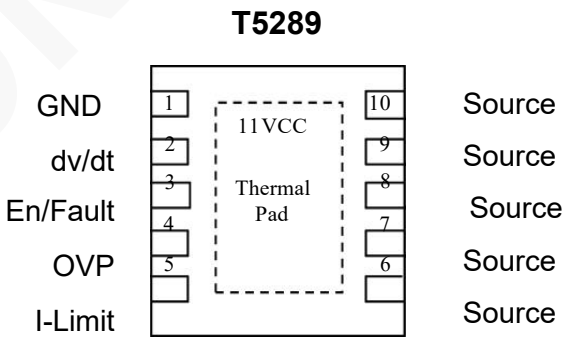
The T5289 can monitoring output current and input voltage. Connected in series to a 4.5V~40V power-rail, it is capable of protecting the electronic circuitry on its output from over current and over voltage during output load transient and input voltage transient. If a continuous short-circuit is present on the board, when power is re-applied, T5289 initially limits the output current to a safe value to lower the power on T5289 and a thermal protection circuit is integrated as well. There is no degradation on T5289 after short-circuit/thermal protection events and it is reset either by recycling the supply voltage or using the En/Fault pin. T5289 also has a programmable delay to control turn on time.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
T5289QE1U	5289	-40°C~+125°C	DFN3X3-10

Note: QE: DFN3X3-10
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



DFN3X3-10

Note: Thermal Pad isthe VCC Pin.

TEL: 86-755-27081036

Absolute Maximum Ratings

Positive power supply voltage (steady state)
VCC.....-0.3V to +45V
Positive power supply voltage (max 100ms)
VCC.....-0.3V to +50V
VOUT/source (max 100ms)..... -0.3V to VCC+0.3V

I-Limit (max 100ms).....V to +50V
En/Fault.....V to +7V
dv/dt.....V to +7V

Thermal Resistance Junction to Ambient, (θJA)
DFN3X3-10..... 340°C/W
Continuous P owe - Di ssip atio n (TA = +2 5°C)
DFN3X3-10..... 1.5W
Operating junction temperature range ◦
..... *D* 5 °C -º) +5 ˢD
Storage Temperature Range..... -65°C to 150°C
Lead temperature (soldering) 10 sec..... 260°C
ECD (HBM).....2 CD
ESD (MM)..... 200V
ESd (CDM).....50+V

(1) The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Electrical Characteristics

(V_{cc} =12V, $V_{En/Fault}$=3.3V, C,=10pF, C_O=47|JF, ^=25°0.

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

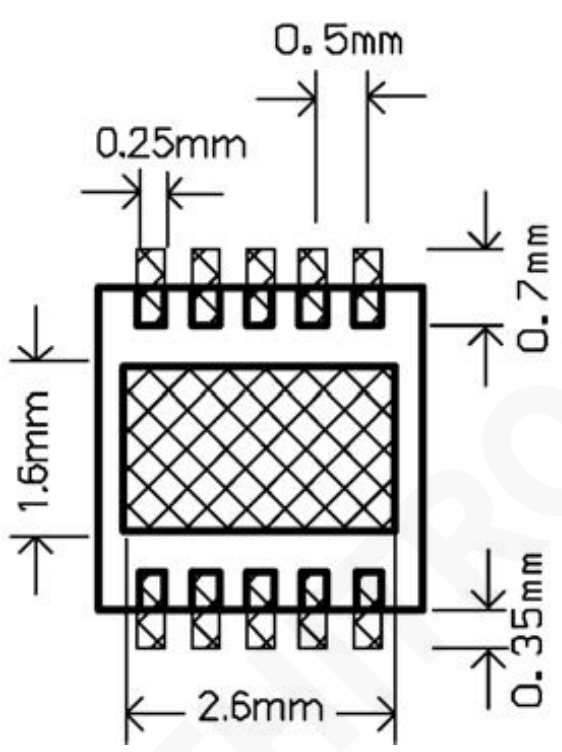
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Under/Overvoltage protection						
Overvoltage threshold	Vciamp		—	1.24	—	V
Under voltage lockout	VjVLO	Turn-on, voltage rising	3.5	3.7	3.9	V
UVLO hysteresis	Vbdyst		—	0.3	—	V
Power MOSFET						
Delay time	TDLY	Enabling of chip to ID = 100mA with an 1A resistive load	—	350	—	MS
ON resistance	RDS_ON	(1)	—	15	—	mQ
		-40°C<Tj< 125°C(2)	—	—	18	
Off state output voltage	VQFF	Vcc-18V, VGs=0, R|=infinite	—	190	300	mV
Continuous current	ID	0.5in²pad, TA=25°C(1)	—	7	—	A
		Minimum copper, TA=80°C	—	3.5	—	
Current limit						
Short-circuit current limit	I Short	RLIMIT = 15Q, SOURCE < 0.5V	—	2	—	A
Hold current limit	I Hold	RLIMIT - 15Q	—	5	—	A
Trip current limit	Lim	RLIMIT - 15Q	—	7.5	—	A
dv/dt circuit						
Output voltage ramp time	dv/dt	Enable to VOUT-1 1-7V, No Cdv/dt	0.5	0.9	1.8	ms

Electrical Characteristics (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
En/Fault						
Low level input voltage	V|L	Output disabled	—	—	0.5	V
Intermediate level input voltage	V|(|NT)	Thermal fault, outputd i sabled	h	th	1.95	V
High level input voltage	V_{IH}	Output enabled	2.5	—	—	V
High state maximum voltage	VI (MAX)		3.4	4.3	5.4	V
Low level input current (sink)	IIL	sh th	—	-16	-25	|JA
Maximum fan-out for fault signal		Total numbers of chips that can be connected to this pin for simultaneous shutdown	—	—	3	Units
Total device						
Bias current	I Bias	Device operational	—	420	—	|JA
		Shutdown	—	360	—	
Minimum operating voltage	Vmin		—	—	3.5	V
Thermal latch						
Shutdown temperature	TSD	(1)	—	165	—	°C

1. Pulse test: Pulse width = 300|_is, Du0 cycle = 2%
2. Guaranteed by design, but not tested in production

Minimum Footprint PCB Layout Section



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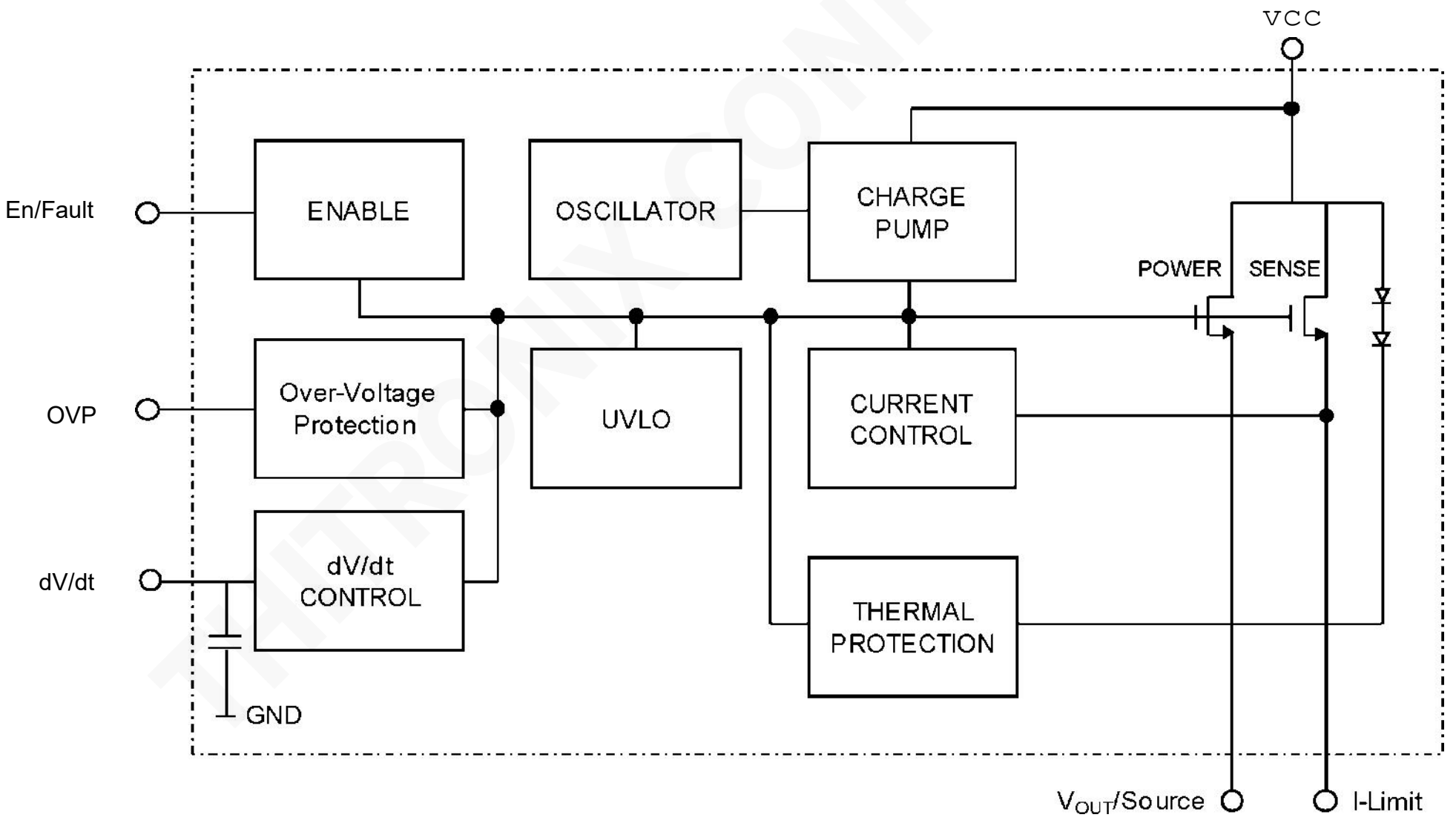
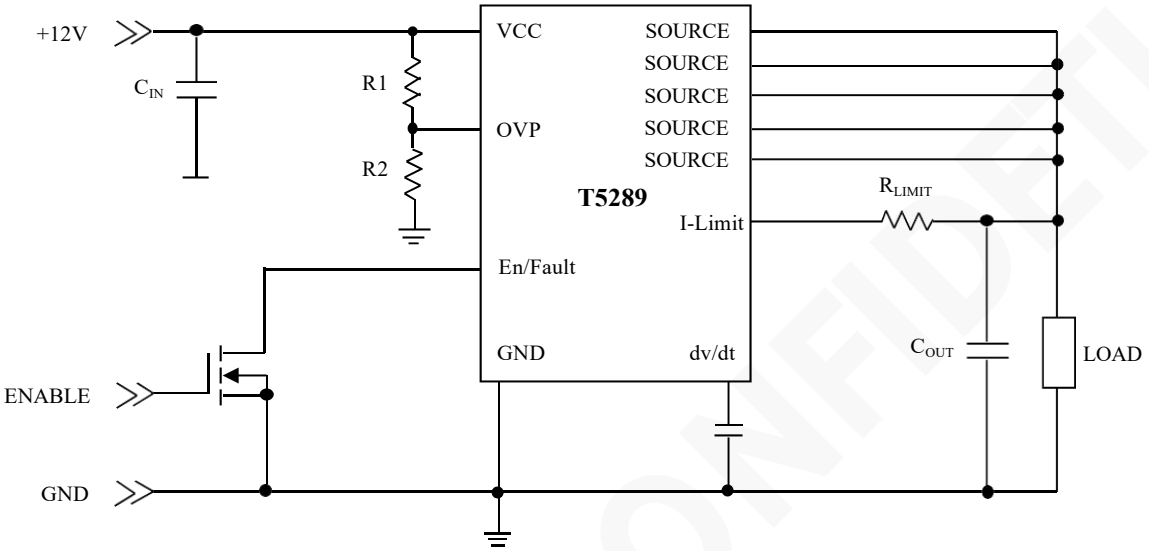
Pin Description

PIN	NAME	FUNCTION
1	GND	Ground pin
2	dv/dt	The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a ramp-up time of around 1 ms. An external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.
3	En/Fault	The En/Fault pin is a tri-state, bi-directional interface. During normal operation the pin must be lef floating, or it can be used to disable the output of the device by pulling it to ground using an oper drain or open collector device. If a thermal fault occurs, the voltage on this pin goes into an intermediate state to signal a monitor circuit that the device is in thermal shutdown. It can be connected to another device of this family to cause a simultaneous shutdown during therma events.
4	OVP	Input over voltage threshold setting input.
5	I-Limit	A resistor between this pin and the Source pin sets the overload and short-circuit current limit levels.
6~10	Source	Connected to the source of the internal power MOSFET and to the output terminal of the fuse
11	VCC	Exposed pad. Positive input voltage must be connected to VCC.

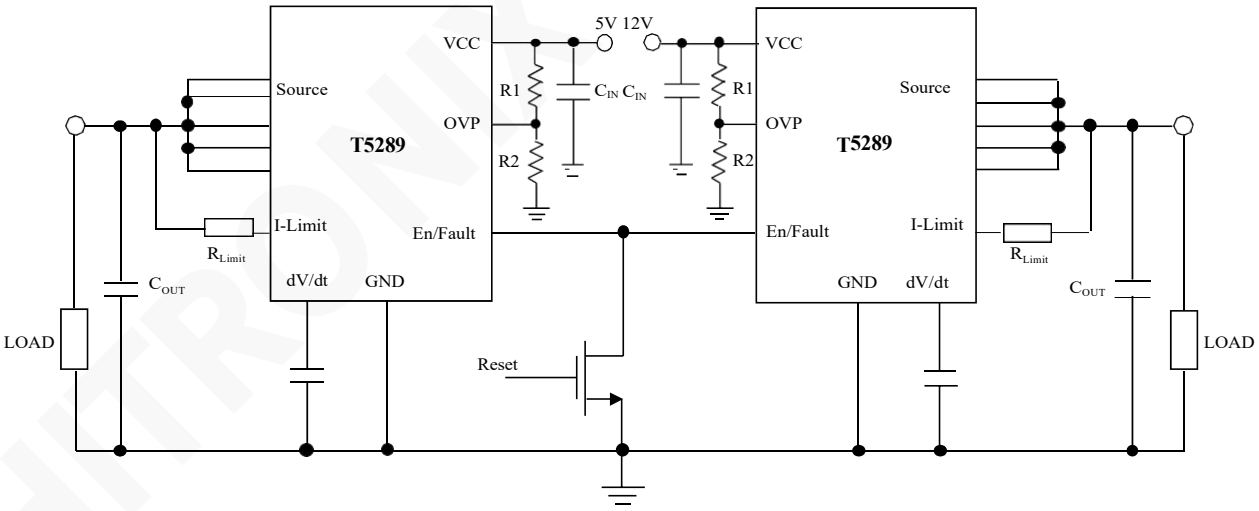
Block Diagram



Typical application



Typical Application Circuit



Typical HDD Application Circuit

Turn-on

When the input voltage is applied, the En/Fault pin goes up to the high state, enabling the internal control circuit. After an initial delay time of typically 350 us, the output voltage is supplied with a slope defined by the internal dv/dt circuit. If no additional capacitor is connected to dv/dt pin, the total time from the Enable signal going high and the output voltage reaching the nominal value is around 1 ms (Fig. 1)

Normal operating condition

The T5289 buffers the circuitry on its output with the same voltage shown at its input, with a small voltage drop due to the N-channel MOSFET resistance.

Current limiting

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET in order to clamp the output current at the value selected externally by means of the limiting resistor RLIMIT which connected between the current limit pin (I-limit) and the load.

Rough formulas for current limiting are shown below:

For trip current,

For hold current,

'Hold

$$\text{Lim} \quad \frac{60}{R_{LIMIT}} + 2.4(A)$$

Cdv/dt calculation

Connecting a capacitor between the dv/dt pin and GND allows the modification of the output voltage ramp-up time. Given the desired time interval At during which the output voltage goes from zero to its maximum value, the capacitance to be added on the dv/dt pin can be calculated using the following theoretical formula:

Equation 1

$$tsiew = 24x\ 106x(50pF + Cdv/\ dt)$$

$$Cdv / dt = \frac{tsiew \_ 50pF}{24x10^{6}}$$

Where Cdv/dt is expressed in Farads and the time in seconds.

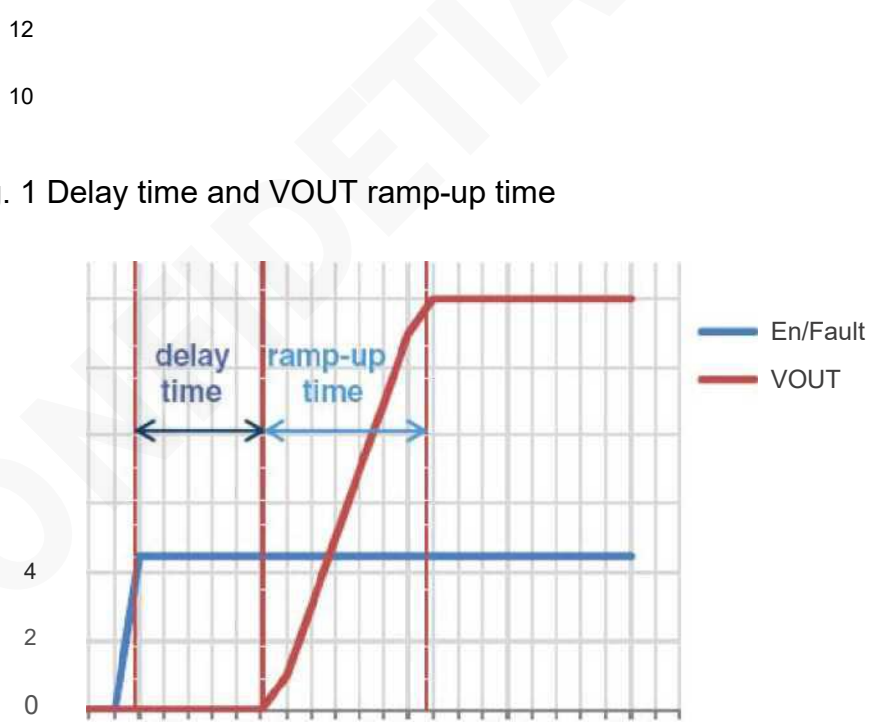


Fig. 1 Delay time and VOUT ramp-up time

Where RLIMIT is expressed in Ohm, and Table1 shows some recommended $R|_{imit}$ with respective current limit value.

Over-Voltage Protection(OVP)

OVP PIN is utilized to set over-voltage threshold according to formula shown below. When OVP PIN is connected to GND, default OVP threshold is 45V. The OVTH is adjustable from 4V to 45V.

VIN OVTH x I ^{R2} | = 1.24

⟶ "R1 + R2 ⌡

Thermal shutdown

If the device temperature exceeds the thermal latch threshold, typically 165 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The En/Fault pin of the device is automatically set at an intermediate voltage, in order to signal the over temperature event. In this condition, T5289 can be reset either by cycling the supply voltage or by pulling down the En/Fault pin below the $V_{,L}$ threshold and then releasing it.

En/Fault pin

The output of the device and, at the same time, of providing information about the device status to the application.

When it is used as a standard Enable pin, it should be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, it turns the output of the protect chipset off.

If this pin is left floating, since it has internal pull-up circuitry, the output of T5289 is hold ON, in normal operating conditions.

In case of thermal fault, the pin is pulled to an inter- hh monitor circuit, informing it that a thermal shutdown has occurred, or it can be directly connected to the En/Fault pins of other devices on the same application in order to achieve a simultaneous enable/disable feature.

When a thermal fault occurs, the device can be reset either by cycling the supply voltage or by pulling down the En/Fault pin below the $V_{,L}$ threshold and then releasing it.

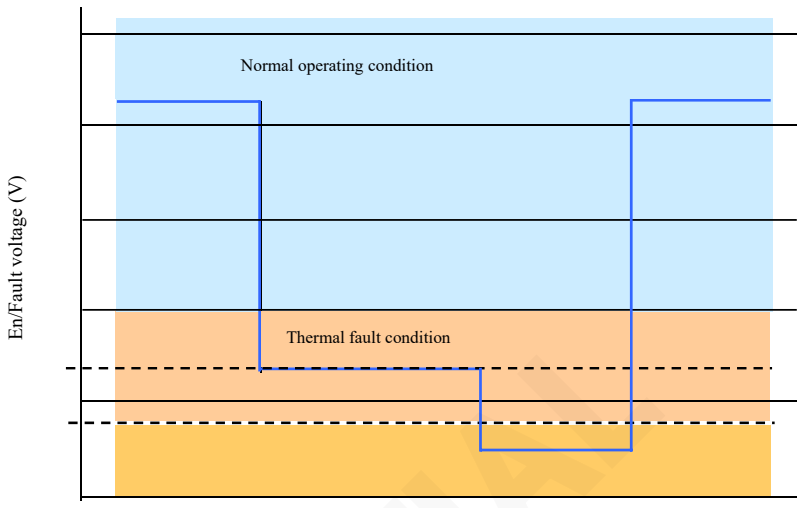
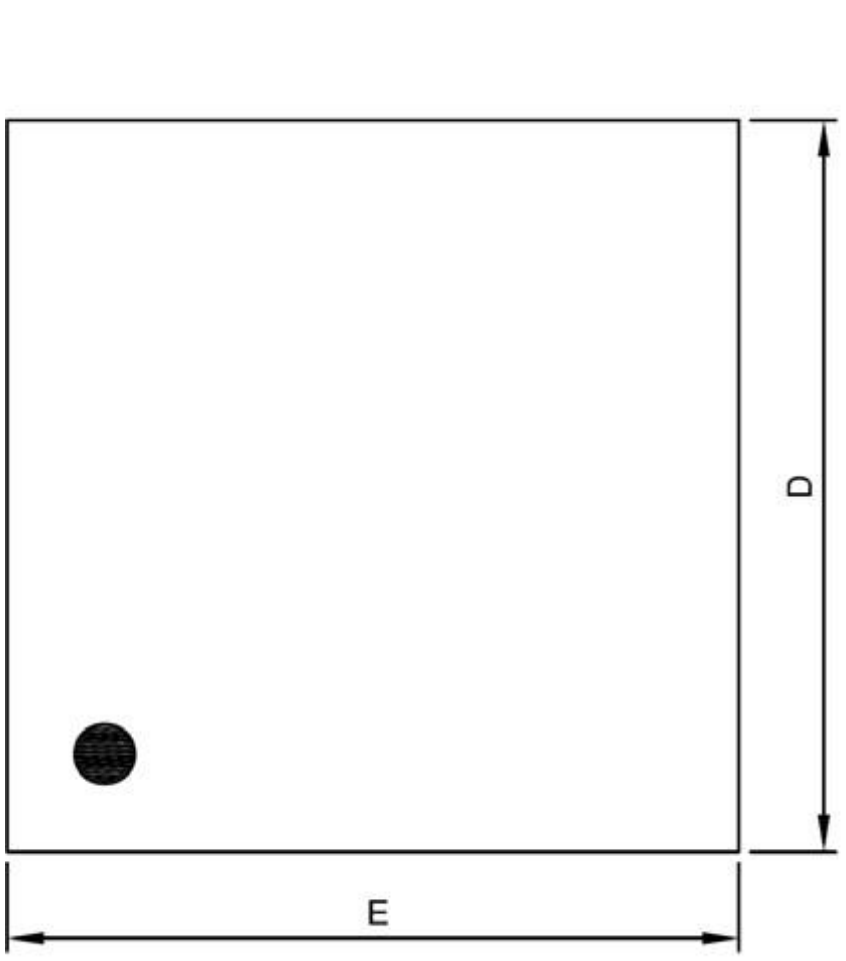


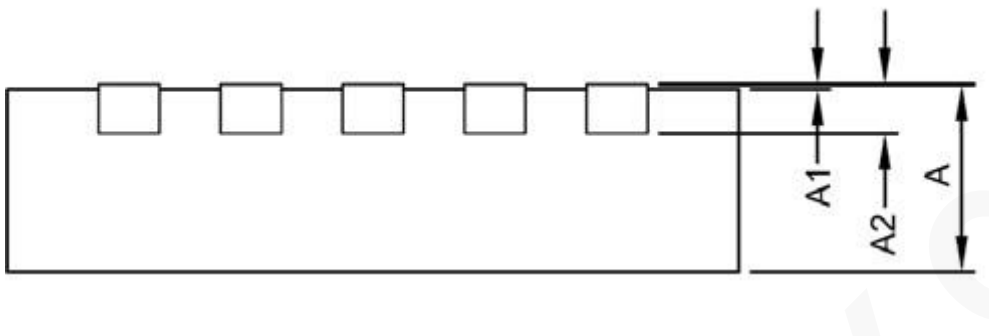
Fig. 2 En/Fault pin status

Table1:Current Limit vs. Current Limit Resistor (VCC=12V)

R_{LIMIT}(Q)	11	13	15	18	22	51	68	100
Trip Current (A)	8.5	7.5	7.1	6.7	6.2	5.2	4.9	4.8
Hold Current (A)	6.5	5.7	5	4.4	3.7	1.9	1.5	1.1

Package Information

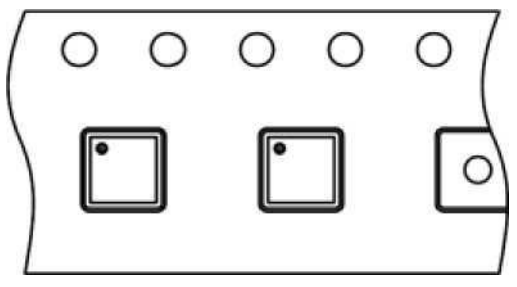




DFN3X3-10 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0,0354	0.0394
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0080 REF		
D	2.95	3.00	3.05	0.1161	0.1181	0.1201
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	0.95	1.00	1.05	0.0374	0.0394	0.0413
E1	2.55	2.60	2.65	0.1004	0.1024	0.1043
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177

Taping Specification



Feed Direction

PACKAGE	QTY/REEL
DFN3X3-10	3,000 ea